AXERA 爱芯元智

AX620Q

AX620Q is an ultra-high definition intelligent IPC SoC developed by Axera for the industrial market. Integrated with the cutting edge AXProton 4.0 AI-ISP, this chip supports 5Mp@30 fps real-time video under blacklight. Equipped with AXNeutron 4.0 high performance optimized NPU engine, AX620Q takes a leading role in the high-quality image processing and analysis. This chip also provides reliable and easy-to-use SDK, empowering users to mass produce effectively.

Features

CPU
- Dual Cortex A53 1.2 GHz
- 32KB I-Cache
- 32KB D-Cache
- 256KB L2 Cache
- Neon acceleration
- Integrated FPU

NPU
- Max. 9.6 TOPs @INT4, and 2.4 TOPs @INT8
- Supports multiple mainstream deep learning framework
- Supports IVE

ISP
- Max. 5Mp@30fps AI ISP
- Supports 3A (AF, AWB, AE)
- Supports AI-3DNR, 3DNR
- Supports AI-RLTM
- Supports 2f HDR
- Supports FPN removal and DPC
- Supports fisheye correction
- Supports DIS and EIS
- Supports defogging
- Supports lens shading

Video Encoding
- H.264 HP/MP/BP Level 5.1
- H.265 MP Level 5.0
- I-/P-frames
- Real-time multi-stream H.264/H.265 encoding: 5Mp@30 fps + 1080p@30 fps + 720p@30 fps
- CBR/VBR/FIXQP bit rate control mode
- 8 ROI encoding
- JPEG snapping performance: 5Mp@40 fps

Video Decoding
- H.264 HP/MP/BP: Level 4.2
- Max. decoding performance: 1080p@60 fps
- I-/P-/B-frames
- JPEG decoding: 1080p@60fps

Video and Image Processing
- Customizable position and number of OSD overlays
- Supports mosaic
- Supports bitmap

Peripherals

Video Interfaces
VI
- 1x4 Lane or 2x2 Lane MIPI
- Up to 2.5 Gbps per lane
- Supports Sub-LVDS

VO
- 1-ch MIPI DSI
- Up to 1080p@60 fps output

Memory Interfaces
SDRAM Interface
- SiP 2Gb LPDDR4
- Up to 2800 Mbps

SPI Flash Interface
- Supports SPI Nor Flash
- Supports SPI Nand Flash

eMMC v5.1 Interface
- Maximum capacity of 2 TB

Ethernet
- One Ethernet ports
- RMII modes
- Internal PHY supports RMII

USB
- One USB 2.0
- Supports Host or Device

Other Interfaces
- I2S codec interface
- I2C, SPIs, and UART

Security
- Secure boot
- Hardware-based encryption and decryption algorithms (including AES, DES, and 3DES)
- Hardware-based HASH algorithms (SHA-1, SHA-224, and SHA-256)

Startup
- Boot from eMMC, SPI Nor Flash, SPI Nand Flash
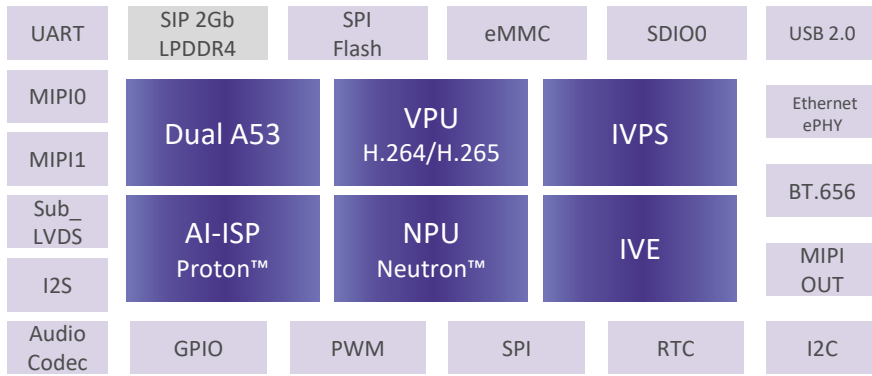
Physical Spec.

Operating Voltage
- 0.8V core voltage
- 1.1V LPDDR4 interface voltage
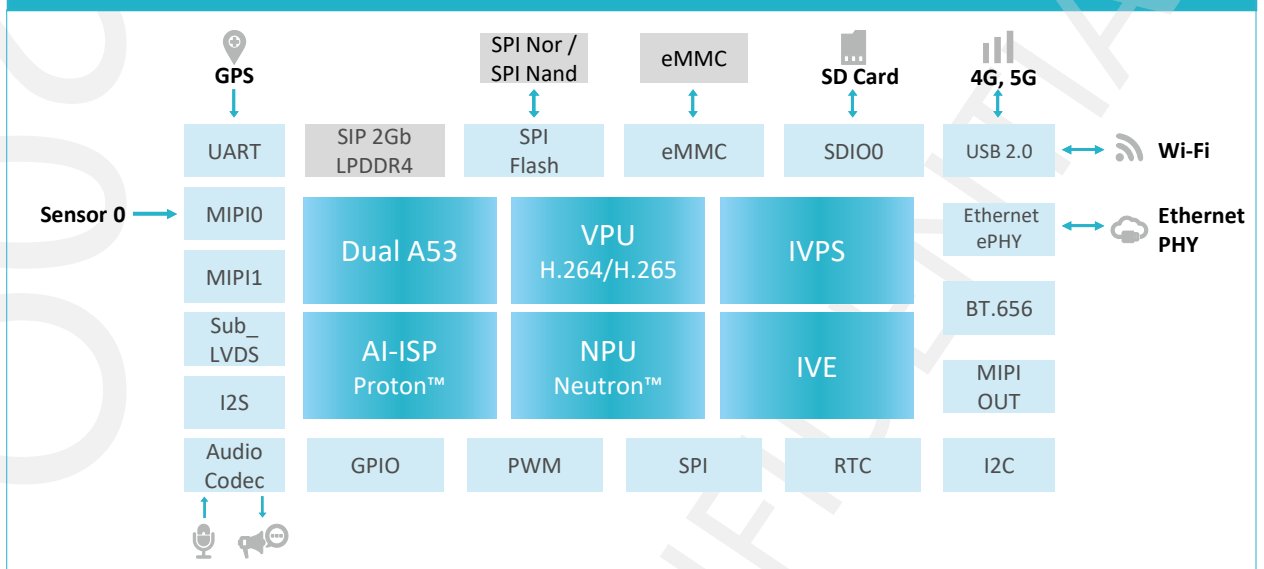- 1.8V/3.3V I/O voltage

Package
- 10 mm × 10 mm TFBGA

AXERA
AX620Q

WeChat Subscription

AXera Official Website

AX620Q Block Diagram

UART	SIP 2Gb LPDDR4	SPI Flash	eMMC	SDIO0	USB 2.0
MIPI0	Dual A53	VPU H.264/H.265	IVPS		Ethernet ePHY
MIPI1					BT.656
Sub_LVDS	AI-ISP Proton™	NPU Neutron™	IVE		MIPI OUT
I2S					
Audio Codec	GPIO	PWM	SPI	RTC	I2C

AI IP Camera Solution

GPS

Sensor 0 →

SPI Nor / SPI Nand   eMMC   SD Card   4G, 5G

UART	SIP 2Gb LPDDR4	SPI Flash	eMMC	SDIO0	USB 2.0	→ Wi-Fi
MIPI0	Dual A53	VPU H.264/H.265	IVPS		Ethernet ePHY	↔ Ethernet PHY
MIPI1					BT.656
Sub_LVDS	AI-ISP Proton™	NPU Neutron™	IVE		MIPI OUT
I2S					
Audio Codec	GPIO	PWM	SPI	RTC	I2C

AX620Q Brief

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