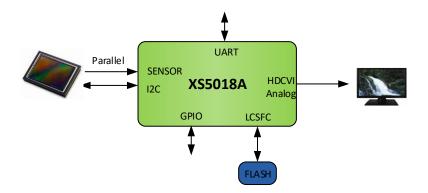
XS5018A is an image signal processing chip designed for CMOS image sensors, specifically tailored for vehicle surround-view cameras. It is mainly targeted at the automotive product market, featuring highly integrated peripheral components to simplify product design. The chip is equipped with a high-performance ISP and 3DNR, offering processing capabilities up to 1080P@30 fps. It supports standard-definition analog output via CVBS (960H) and high-definition analog output through HDcctv 720P, 960P, and 1080P. With an embedded CPU, XS5018A enables flexible software applications.

- O Inventor of coaxial HD, with proprietary intellectual rights
- Integrated DAC, video buffer, and comparator
- **© Compatible with HDcctv and CVBS**
- © Supports 960H, 720p, 960p, and 1080p
- ◎ ISP supports up to 1080p@30 fps
- **©** High-performance 2D and 3D noise reduction
- **O** Supports seamless frame rate reduction



Video Input Interface

- Supports 10bit RGB Byer input and clock up to 100 MHz
- External Interface
- Supports POR
- UART × 1, can be multiplexed as GPIO
- I2C × 1
- SPI × 1, can be multiplexed as GPIO
- Integrated with JTAG, can be multiplexed as GPIO
- Integrated with a comparator
- Integrated with video DAC and Buffer
- Image Signal Processing
- Supports 2D noise reduction
- Supports 3D noise reduction
- Supports shading correction and dynamic bad pixel correction
- Supports AE and AWE
- Supports correcting uneven green
- Supports color correction and false color correction

- Supports edge enhancement
- Supports seamless frame reduction
- Video Processing
- Supports video cropping and scaling up/down
- Supports privacy masking and OSD overlay
- Physical Specifications

Core voltage: 1.1 V

Common IO voltage: 3.3 V

Sensor IO voltage: 1.8/3.3 V

QFN5X5, 48-pin, pitch of 0.35 mm

It supports various coaxial HD and SD formats, including

960H@25/30 fps

720P@25/30/50/60 fps

960P@25/30 fps

1080P@25/30 fps

 Integrated with a video DAC, video buffer, and comparator, further simplifying PCB design and reducing hardware BOM costs