XS2120

Controller Integrated with PD and DC/DC Based on the IEEE 802.3AF/AT Standard Integrated Power MOSFET V1.0

Product Overview

XS2120 is a controller that integrates both Power Device (PD) and DC/DC functionalities based on the IEEE 802.3af/at standard. The PD controller provides a complete power interface for PD in PoE systems. It offers detection signals, classification signals, and an integrated isolated power MOSFET with surge current control. The integrated power MOSFET has a voltage rating of 100 V, an on-resistance of 0.65 Ω, and supports working current up to 800 mA. It also features undervoltage protection and over-temperature protection, along with wide hysteresis and long-duration pulse shielding to compensate for the resistive attenuation of twisted-pair cables, ensuring interference-free transmission during power-on and power-off. The DC/DC controller integrates a 200V power MOSFET and uses a Primary-Side Regulation (PSR) method, suitable for Flyback topology. It features built-in high-precision constant current and constant voltage control technology, along with optimized valley switching technology. The output current error is within 3%, and the output voltage error accuracy can reach 2%. The switching frequency of up to 70 kHz allows the design to use relatively small transformer sizes. The multi-segment curve control operation mode with PWM, PFM, and PBM modes further optimizes system conversion efficiency under different loads while effectively reducing noise.

XS2120 detects the connection status of a wall adapter power source, enabling seamless switching from PoE power to wall adapter power. Additionally, XS2120 provides a power good (PG) signal and fold-back thermal protection. XS2120 features short-circuit protection and open-loop protection, ensuring high system efficiency and good EMI characteristics. XS2120 is housed in a QFNWB5x5-32L-AN package and operates over an extended temperature range from -40 °C to 105 °C.

Features

PD Controller

- Compatible with IEEE 802.3af/at PD power interface
- Integrated with 100V, 0.4Ω isolated power MOSFET
- Undervoltage protection
- Over temperature protection
- MOSFET supports current of 800 mA
- Surge current limit of 180 mA
- Wall power switching with output signal indication
- Current limiting and fold-back protection
- PG signal output

DC/DC Controller

- Primary-side control mode
- Integrated with high-voltage MOSFET switch of 200 V
- Maximum peak output power of 16 W
- Output current accuracy of 3%
- Output voltage accuracy of 2%
- Integrated with active cycle resonant technology
- Built-in output short-circuit protection and loop open protection
- Output overvoltage protection
- Over-temperature protection
- Valley switching technology for low switching losses
- Low-frequency start characteristics to optimize startup performance

Typical Application

- Video Security
- VoIP
- Wireless AP
- PoE splitter

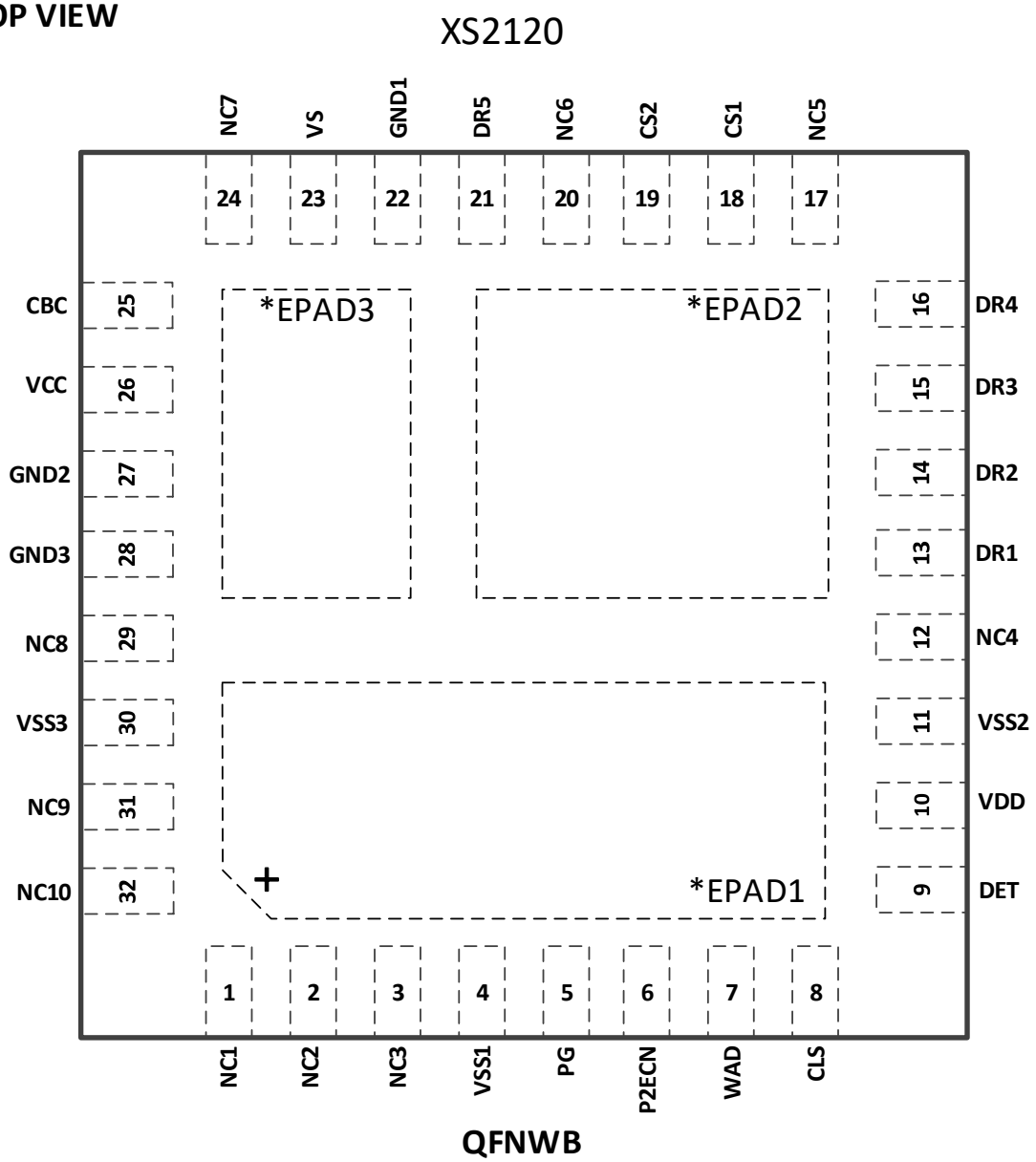
Order Information

PART	TEMP RANGE	PIN-PACKAGE
XS2120	-40 °C to 105 °C	QFNWB5 × 5-32L-AN

QFNWB5 × 5-32L-AN
(5.00 mm × 5.00 mm)

Pin Arrangement

TOP VIEW



QFNWB

* EPAD1 externally connected to VSS * EPAD2 externally connected to DR * EPAD3 externally connected to GND

Pin Description

Pin	Name	Features
1/2/3/12/17/20/24/29/31/32	N.C.	No Connection. Internally disconnected. Leave floating during use.
4/11/30	VSS	PD negative power input. VSS is connected to the source of the integrated isolated N-channel MOSFET.
5	PG	PD power good open-drain output. When the integrated isolated NMOSFET switch is on, PG absorbs 230 μA of current to disable subsequent DC-DC conversion until NMOSFET is fully on. In detect, classify, and regulated supply modes, prevent PG from drawing current.
6	P2ECN	Active low, dual-event classification detection or wall adapter detection output. Enables 1.5mA current draw at P2ECN when performing dual-event classification or when a wall adapter is present. After isolation NMOSFET is fully open during dual-event classification, P2ECN enables current draw and locks as low until VDD falls below the UVLO threshold. When wall adapter power (typically over 9 V) is applied between WAD and GND, P2ECN is also active. P2ECN is not locked when triggered by WAD.
7	WAD	Wall adapter detector input. Enables wall adapter detection when VDD - VSS exceeds the event threshold. Detection occurs when the voltage between WAD and GND exceeds 9V. Disconnects isolated N-channel power MOSFET and enables P2ECN current draw circuit when a wall adapter is connected. Connect WAD directly to GND when not using a wall adapter or other auxiliary power.
8	CLS	Classification resistor input. Connect a resistor (R_{CLS}) between CLS and VSS to set the required classification current. For specific PD classification corresponding resistor values, refer to the classification current indicators in the datasheet.
9	DET	Detection resistor input. Connect a characteristic resistor (R_{DET} = 24.9 kΩ) between DET and VDD.
10	VDD	PD positive power input. Connect a bypass capacitor of 68 nF (minimum) between VDD and VSS.
13/14/15/16/21	DR	Drain of the 200V power NMOSFET.
18/19	CS	DC/DC controller peak current sampling pin.
22/27/28	GND	Ground for the DC/DC controller. Internally known as RTN for the PD controller.
23	VS	DC/DC controller feedback input pin.
25	CBC	Cable voltage drop compensation adjustment pin, allows for compensation of the output voltage drop, typically connect a fixed resistor value (usually 200 kΩ).
26	VCC	Supply voltage for the DC/DC controller.
33	EPAD1	Bottom thermal pad, externally connect to VSS.
34	EPAD2	Bottom thermal pad, externally connect to DR.
35	EPAD3	Bottom thermal pad, externally connect to GND.

Zhejiang Chipup Electronics Co., LTD

Address: 1168 Bin’an Road Binjiang District Hangzhou Zhejiang, China

Official website: www.chipup.com

Zip code: 310053