XS2180A

Quad, Compatible with IEEE 802.3 at/af

Ethernet PSE Controller

User Manual

Updates and Modifications

To enhance the security of this product and to provide you with a better user experience, Chipup may improve the product through automatic software updates without prior notice and without any liability.

Chipup reserves the right to modify any information in this document at any time. Changes will be incorporated into new versions of this document without further notice. There may be slight differences in some features of the product before and after updates.

1 Overview

1.1 Product Overview

XS2180A is a quad, power sourcing equipment (PSE) power controller designed for use in IEEE® 802.3at/af-compliant PSE. This device provides Power Device (PD) detection, classification, current limiting, and load disconnection detection. It supports both fully automatic operation and software programmability. The device also supports 2-event classification and Class 5 for detection and classification of high-power PDs. Its single power supply delivers up to 70W per port (Class 5 enabled) and provides large capacitance detection for legacy PDs.

I²C-compatible 3-wire serial interface for software configuration and programming offers real-time current and voltage readings for each port. Enhanced programmability increases design flexibility and provides field diagnostics for various non-standard system applications.

The device is available in a space-saving, 32-pin QFN32L (5 mm × 5 mm) and is rated for the automotive (from -40 °C to +105 °C) temperature range.

1.2 Features

- Compatible with IEEE 802.3 at/af
- Current sensing resistor of 0.25Ω
- Up to 70W per port
- 9-bit real-time monitoring of port current and voltage
- Supports I²C
- Supports single-supply operation
- Supports DC load disconnection detection
- Over-temperature protection
- 32-PIN QFN32L (5 mm × 5 mm) power package

1.3 Applications

- Switches/Routers
- Midspan power injectors

1.4 Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
XS2180A	-40 °C to 105 °C	QFNWB5 × 5-32L

2 Application Diagram

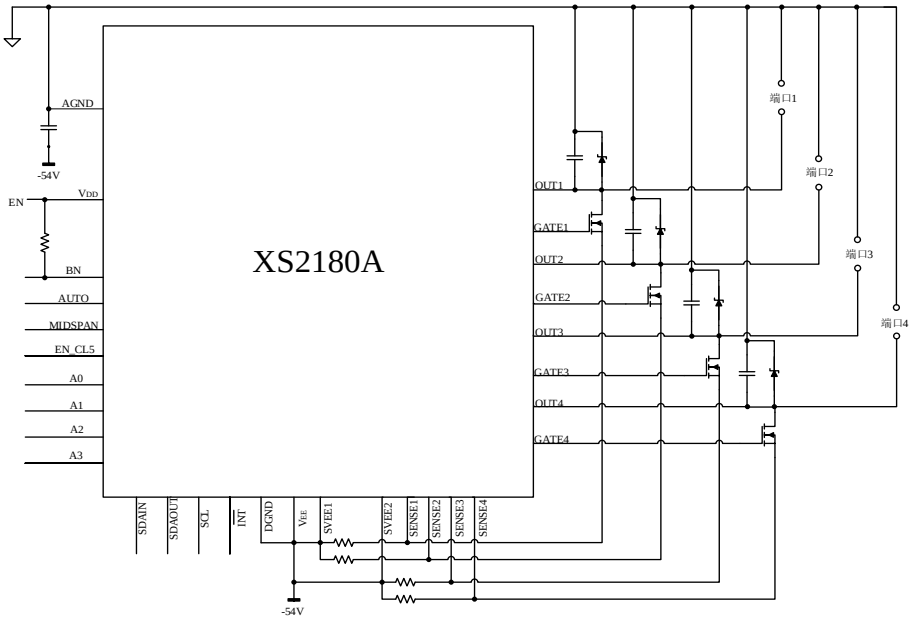

Figure 1 Schematic

3 Revision History

Date	Version	Revision
October 2024	V1.0	Updated the format of the document.

4 Pin

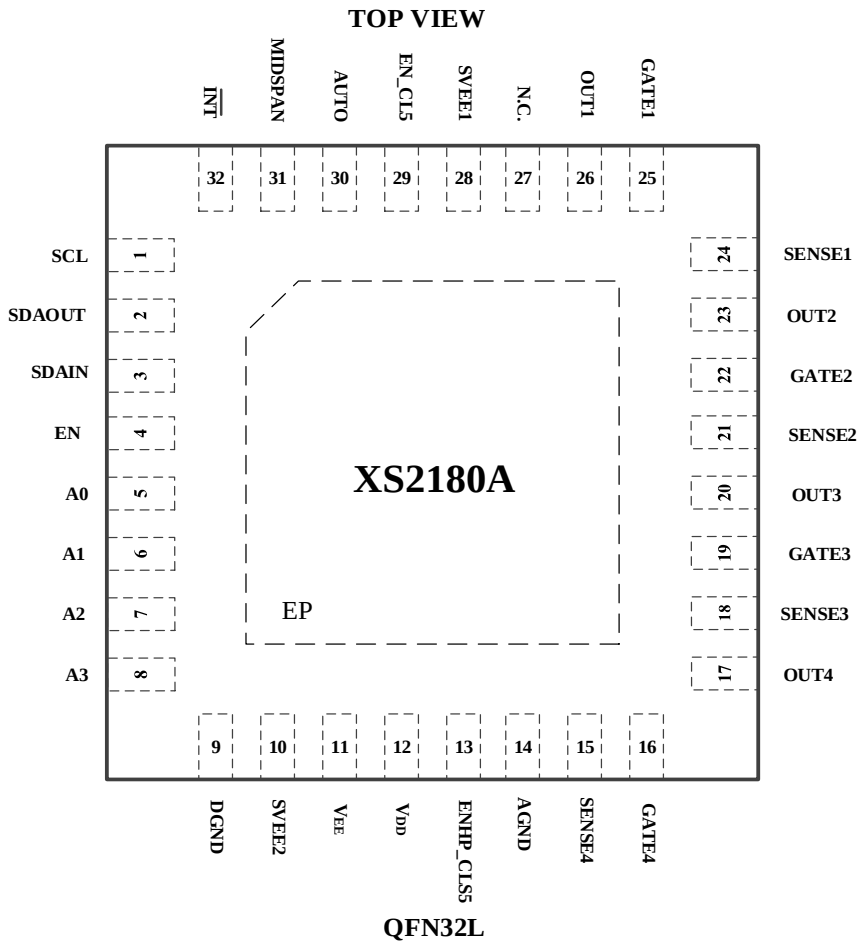

Figure 2 XS2180A QFN32L Package Pin Arrangement

Table 1 Pin Description

Pin		I/O	Description
Name	NO.		
SCL	1	I	Serial interface input clock line. Reference DGND. Connect to DGND if I^2C interface is unused.
SDAOUT	2	OD	Serial interface data output line. Reference DGND. Connect to DGND if I^2C interface is unused.
SDAIN	3	I	Serial interface data input line. Reference DGND. Connect to DGND if I^2C interface is unused.
EN	4	I	Enable input. Reference DGND. For normal operation, connect to V_{DD} via an external pull-up resistor. For more details, refer to Section 8.3.17.

A0, A1, A2, A3	5/6/7/8	IL	Correspond to slave address bits 0, 1, 2, and 3 respectively. Slave address format: bits 3, 2, 1, 0 correspond to device address (0:1:0:A3:A2:A1:A0; see Table 9). Pull up the slave address internally to V_{DD}. The default address (0101111) is used if left floating. Address is locked after power-up or reset.
Pin		**I/O**	**Description**
Name	**NO.**		
DGND	9	P	Digital ground. Connect externally to V_{EE}.
SVEE2	10	P	Negative input for current detection on ports 3/4. Use Kelvin sensing on PCB layout for optimal current detection accuracy.
V_{EE}	11	P	Analog ground. Connect to AGND via a 100V, 0.1μF ceramic capacitor.
V_{DD}	12	P	Digital power output. Connect an RC network. For more details, refer to the section for V_{DD}.
ENHP_CLS5	13	IL	Non-standard high-power CLS 5 control enable; internally pulled down to ground, not enabled. After being externally pulled up to V_{DD}, PSE can implement Class 5 grading without connecting to the non-standard PD, achieving 70W non-standard power supply.
AGND	14	P	Analog power input.
SENSE 4, 3, 2, 1	15/18/21/24	I	Positive input for current detection. Connected to the source terminal of the external power MOSFET. A 0.25Ω current detection resistor is placed between SENSE and SVEE. Use Kelvin sensing on PCB layout for optimal current detection accuracy.
GATE 4, 3, 2, 1	16/19/22/25	O	Corresponding to the gate drive terminal of the external power MOSFET for each port (see typical working circuit for details).
OUT 4, 3, 2, 1	17/20/23/26	I/O	Output voltage detection for each port.
N.C.	27		No internal connection. Leave floating during use.
SVEE1	28	P	Negative input for current detection on ports 1/2. Use Kelvin sensing on PCB layout for optimal current detection accuracy.
EN_CL5	29	I	Class 5 enable input. Reference DGND. Pull down EN_CL5 to DGND internally. Float this pin to disable the classification of Class 5 devices (IEEE 802.3at-compatible mode). EN_CL5 is connected to V_{DD} for the classification of Class 5 devices. EN_CL5 is locked after power-up or reset.
AUTO	30	IL	Automatic/Shutdown mode input. Reference DGND. AUTO is internally pulled up to V_{DD}. If floating, system defaults to automatic mode. Connect to DGND to default to shutdown mode. Device mode can be changed by software. AUTO is locked after power-up or reset.
MIDSPAN	31	IL	Mid-span mode logic input. Reference DGND. MIDSPAN is internally pulled up to V_{DD}. If floating, mid-span mode is enabled; connect to DGND to disable mid-span function. MIDSPAN is locked after power-up or reset.
INT	32	OD	Open-drain interrupt output. Reference DGND. Any interrupt pulls INT low. For more details, refer to Section 8.3.13. Connect INT to DGND if I^2C interface is disabled.
EP		P	Externally connect to V_{EE}.

Table 2 IO Type

Type	Description	Type	Description
P	Power or ground	O	Output
I	Input	OD	Open drain output
IL	Input, locked after power-up or reset	N.C.	Not connected.