Introduction to AX520CD

AX520CD is a digital SoC designed for modular IPC market. This powerful chip supports dual-channel HD CMOS sensor inputs, providing superior image processing capabilities through advanced ISP and video pre-processing technologies. With a maximum encoding capacity of 3072×1728@30fps + D1@30fps, AX520CD ensures high-quality multi-stream output.
At its core, AX520CD features an integrated CPU and a light CNN hardware acceleration unit. It enables a wide range of AI-based analysis applications, including human detection, vehicle detection, and facial recognition, making it ideal for comprehensive security solutions.
AX520CD also comes equipped with a variety of integrated modules such as POR, RTC, audio codec, USB 2.0 OTG, and EPHY. Additionally, it includes 128MB of embedded DRAM, and supports commonly used peripheral interfaces like I2C, SPI, SDIO, and UART. It also offers the capability to output standard peripheral operating clocks, and supports fast boot and AOV.

Processor
- ARM Cortex-A7 @ 1Ghz, 32KB I-Cache, 32KB D-Cache
- Integrated FPU. Supports NEON acceleration.

Video Encoding
- Real-time multi-stream H.265/H.264 encoding capability: Up to (3072 × 1728 + 720 × 576)@30 fps
- Encoding frame rate of 1 to 60 fps. Supports CBR/VBR bitrate control.
- Supports ROI encoding
- Supports smart encoding

JPEG Encoding
- Supports JPEG Baseline encoding: Snapping up to 3072 × 1728@30 fps

Audio Encoding
- Supports audio codec of G711, G726, and AAC

Video and Image Processing
- Supports frame rate control of 1 to 60 fps
- Supports image cropping and scaling from 1/16x to 16x
- Supports privacy masking for up to 8 independent regions
- Supports OSD and BMP graphic overlay
- Supports image rotation and flipping (mirroring)

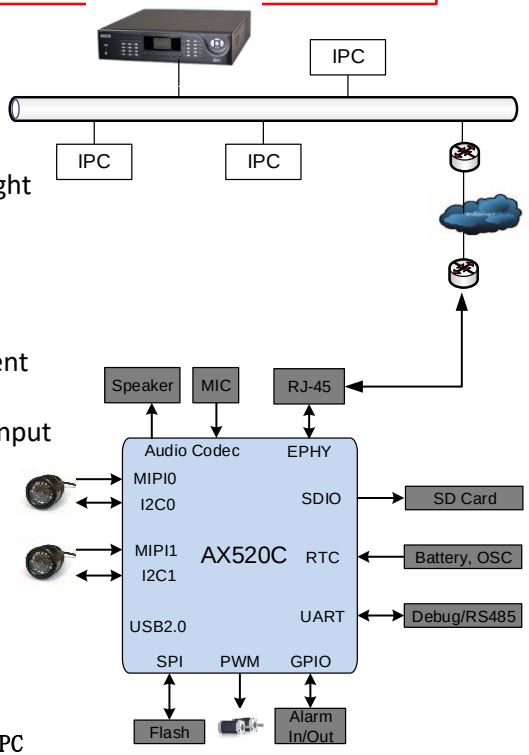
ISP
- Supports static & dynamic bad pixel correction and black level correction
- Supports 2D and 3D noise reduction
- Supports digital gain control, lens shading correction, and strong light suppression
- Supports 3A statistics
- Supports LWDR and 2-frame true WDR synthesis
- Supports GIC, color correction, and GAMMA correction
- Supports edge enhancement, defogging, and digital light supplement

Video Interface
- Supports 1 × 4 or 2 × 2 lane MIPI interface and parallel interface input
- Supports 10/12 Bit Bayer format

Audio Interface
- Built-in audio codec. Supports up to 16-bit, 48kHz sampling.
- Supports I2S interface for external audio codec

Network Interface
- Built-in 10/100M Ethernet PHY

Packaging
- 9 mm × 9 mm and QFN92



IPC

AX520CE vs. AX520CD

Specs		AX520CE	AX520CD
Compact System	CPU	A7@1 GHz Neon/FPU	A7@1 GHz Neon/FPU
	DRAM	DDR2 64 MB	DDR3 128 MB
	Flash	SPI-Nor/Nand Flash, eMMC	SPI-Nor/Nand Flash, eMMC
Intelligent Analysis	MAC Computing Capability	0.5Tops	0.5Tops
Video IN	VI Interface	1 × 4/2 × 2lane MIPI @1.5 Gbps Resolution up to 2880 × 1620	1 × 4/2 × 2lane MIPI @1.5 Gbps Resolution up to 3072 × 1728
Network	Net Interface	10/100M Ethernet PHY	10/100M Ethernet PHY
Peripheral Interfaces	Peripheral Interfaces	USB2(H/D), SDIO, SPI, I2C, UART, GPIO, ADC, and PWM	USB2(H/D), SDIO, SPI, I2C, UART, GPIO, ADC, and PWM
VENC	H265/H264	Supports up to (2880 × 1620 + D1)@30 fps	Supports up to (3072 × 1728 + D1)@30 fps
Other Modules	Packaging	9 mm × 9 mm and QFN92	9 mm × 9 mm and QFN92